**DAILY ASSESSMENT FORMAT**

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| **Date:** | **02-06-2020** | **Name:** | **Varun G Shetty** |
| **Course:** | **DIGITAL DESIGN USING HDL** | **USN:** | **4AL17EC093** |
| **Topic:** | **1.FPGA Basics: Architecture, Applications and Uses.**  **2. Verilog HDL Basics by Intel.**  **3. Verilog Testbench code to verify the design under test (DUT)** | **Semester & Section:** | **6th & ‘B’** |
| **GitHub Repository:** | **Varunshetty4** |  |  |

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| **FORENOON SESSION DETAILS** |
| **Image of session** |
| **Report – Report can be typed or hand written for up to two pages.**  **FPGA Basics: Architecture, Applications and Uses**  **FPGA Architecture**     * *Figure 2: A simplified CLB: The four-input LUT is formed from two three-input units. (Image source: Wikipedia)* * The number and arrangement of components in the CLB varies by device; the simplified example in Figure 2 contains two three-input LUTs (1), an FA (3) and a D-type flip-flop (5), plus a standard mux (2) and two muxes, (4) and (6), that are configured during FPGA programming. * This simplified CLB has two modes of operation. In normal mode, the LUTs are combined with * Current-generation FPGAs include more complex CLBs capable of multiple operations with a single block   **Figure 3:**   * *The Cyclone V SoC internal block diagram (Image Source: Cornell University)* * At the other end of the scale, the Stratix 10 SX targets high-performance applications in communications, data centre acceleration, high-performance computing (HPC), radar processing and ASIC prototyping; that FPGA includes a quad-core 64-bit Arm Cortex-A53 running at up to 1.5 GHz.   **FPGA Design**  FPGA design flow chart, behavioral synthesis, simulation and ...   * *Figure 4: Sample VHDL code for a signed adder* * Once the FPGA design has been created and verified using HDL, the compiler takes the text-based file and generates a configuration file that contains information on how the components should be wired together.   **FPGA Applications:**   * Many applications rely on the parallel execution of identical operations; the ability to configure the FPGA’s CLBs into hundreds or thousands of identical processing blocks has applications in image processing, artificial intelligence (AI), data center hardware accelerators, enterprise networking and automotive advanced driver assistance systems (ADAS). * Many of these application areas are changing very quickly as requirements evolve and new protocols and standards are adopted. FPGAs enable manufacturers to implement systems that can be updated when necessary.   **FPGA History: What Comes Next?**   * The exponential growth of data, and the emergence of fast-changing fields such as AI, machine learning, HPC and genomics, require architectures that are fast, flexible and adaptable. FPGAs are well-positioned to take advantage of these new opportunities.   **Implement a 4:1 MUX and write the test bench code to verify the module**  module top;  wire out;  reg a;  reg b;  reg c;  reg d;  reg s0, s1;  m41 name(.out(out), .a(a), .b(b), .c(c), .d(d), .s0(s0), .s1(s1));  initial  begin  a=1'b0; b=1'b0; c=1'b0; d=1'b0;  s0=1'b0; s1=1'b0;  #500 $finish;  end  always #40 a=~a;  always #20 b=~b;  always #10 c=~c;  always #5 d=~d;  always #80 s0=~s0;  always #160 s1=~s1;  always@(a or b or c or d or s0 or s1)  $monitor("At time = %t, Output = %d", $time, out);  endmodule; |